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EXAMINER	
SHERMAN, STEPHEN G	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/659,593	LEE, BAEK-WOON	
	Examiner	Art Unit	
	Stephen G. Sherman	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,11 and 13-39* is/are pending in the application.

4a) Of the above claim(s) *4-6,19-32,34,35,37 and 38* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,7-9,11,13,14,18,33,36 and 39* is/are rejected.

7)☒ Claim(s) *15-17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed 31 July 2007. Claims 1-9,11 and 13-39 are pending. Claims 4-6,19-32,34,35,37 and 38 have been withdrawn from consideration and claims 10 and 12 have been cancelled.

Response to Arguments

2. Applicant's arguments with respect to claims 1-3,7-9,11,13,14,18,33 and 36 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1-3, 7-9, 11, 36 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawano et al. (US 6,985,194) in view of Tsutomu (JP 2001-296523).

Regarding claim 1, Kawano et al. disclose a display device comprising:

a plurality of pixels, each pixel including a pixel electrode and a switching element (Figure 1 shows TFT 9-2 and pixel electrode 5);

a plurality of gate lines extending in a first direction for transmitting a gate signal to the switching elements (Figure 1 shows scanning lines 11-2), wherein a first portion of each gate line has a first line width larger than a width of other portions of the respective gate line to form a gate electrode (Figure 1 shows scanning line 11-2 which has a first portion of a first line width that is larger to form gate electrode 12.); and

a plurality of data lines extending in a second direction for transmitting data signals to the switching elements (Figure 1 shows signal line 31-1), wherein a first portion of each data line has a first line width larger than a width of other portions of the respective data line to form a source electrode (Figure 1 shows signal line 31-1 which as a first portion of a first line width that is larger to form drain electrode 32, which, as is well known in the display art, could also be the source electrode.),

wherein a second portion of at least one of the gate lines and the data lines has a second line width larger than a width of other portions of the respective gate and data lines and smaller than the first line width of the respective gate and data lines (Figure 1 shows signal line 31-1. The signal line 31-1 can be seen in the Figure 10 have a thick width portion formed where the drain electrode is formed as explained above. The line 31-1 can also be seen to have a thick width portion just below the portion for the drain electrode where the signal line intersects the scanning line 11-2. This portion can be seen to be thinner in width than the drain electrode portion while having a thicker width than the rest of the signal line 31-1.).

Kawano et al. fail to teach the display device comprising a plurality of pixels including color pixels and a white pixel.

Tsutomu discloses of a display device comprising a plurality of pixels including color pixels and a white pixel (Figure 1).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to make the display, in which the data lines have a second portion that has a line width larger than other portions of the lines at every pixel, taught by Kawano et al. have color pixels and a white pixel as taught by Tsutomu, such that all of the color pixels and white pixels would have the larger line width portions, in order to improve the brightness and color reproducibility of the display.

Regarding claim 2, Kawano et al. and Tsutomu disclose the display device of claim 1.

Tsutomu also discloses wherein the three primary color pixels include red, green and blue pixels (Fig. 1).

Regarding claim 3, Kawano et al. and Tsutomu disclose the display device of claim 2.

Tsutomu also discloses a display wherein the green pixel is spaced apart from the white pixel (Fig. 1).

Regarding claim 7, Kawano et al. and Tsutomu disclose the display device of claim 1.

Tsutomu also discloses a display wherein the pixels are arranged in sequence along the first direction (Fig. 1).

Regarding claim 8, Kawano et al. and Tsutomu disclose the display device of claim 7.

Tsutomu also discloses a display wherein the color pixels include red, green and blue pixels and the red pixel, the green pixel, the blue pixel, and the white pixel are arranged in sequence (Fig. 1).

Regarding claim 9, Kawano et al. and Tsutomu disclose the display device of claim 1.

Tsutomu also discloses a display wherein the color pixels have substantially equal size (Fig. 1).

Regarding claim 11, Kawano et al. and Tsutomu disclose the display device of claim 10.

Kawano et al. also discloses wherein the gate lines intersect the data lines (Figure 1) and the at least one portion having the larger line width does not directly intersect other larger line width portions of the respective gate and data lines (Figure 1 shows that the larger line width portion of the signal lines 31 and 31-1 does not directly intersect other larger line width portions of the gate lines 11-2.).

Regarding claim 36, Kawano et al. and Tsutomu disclose the display device of claim 1.

Tsutomu also discloses wherein the white pixel is smaller than the three primary color pixels (Fig. 1).

Regarding claim 39, Kawano et al. and Tsutomu disclose the display device of claim 1.

Kawano et al. also disclose wherein the second portion of the at least one of the gate lines and the data lines does not correspond to a gate or drain electrode (Figure 1 shows that the second portion as described in the rejection of claim 1, does not correspond to a gate or drain electrode.).

6. Claims 13 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawano et al. (US 6,985,194) in view of Tanioka (US 5,929,843).

Regarding claims 13 and 33, Kawano et al. disclose a device and method of driving a display device (Figure 1) comprising:

a plurality of dots (Figure 1, where 5-2 is a dot),

a plurality of gate lines for transmitting gate signals to the pixels (Figure 1 shows scanning lien 11-2), and

a plurality of data lines for transmitting data signals to the pixels (Figure 1 shows signal lines 31 and 31-1),

wherein a first portion of each gate line has a first line width larger than a width of other portions of the respective gate line to form a gate electrode (Figure 1 shows scanning line 11-2 which has a first portion of a first line width that is larger to form gate electrode 12.),

a first portion of each data line has a first line width larger than a width of other portions of the respective data line to form a source electrode (Figure 1 shows signal line 31-1 which as a first portion of a first line width that is larger to form drain electrode 32, which, as is well known in the display art, could also be the source electrode.) and

a second portion of at least one of the gate lines and the data lines has a second line width larger than a width of other portions of the respective gate and data lines and smaller than the first line width of the respective gate and data lines (Figure 1 shows signal line 31-1. The signal line 31-1 can be seen in the Figure 10 have a thick width portion formed where the drain electrode is formed as explained above. The line 31-1 can also be seen to have a thick width portion just below the portion for the drain electrode where the signal line intersects the scanning line 11-2. This portion can be seen to be thinner in width than the drain electrode portion while having a thicker width than the rest of the signal line 31-1.).

Kawano et al. fail to teach a device and method comprising a plurality of dots, each dot including red, green, blue, and white pixels, the device comprising: a gate driver supplying the gate signals to the gate lines; a data driver supplying the data voltages to the data lines; and an image signal modifier for converting three-color image signals into four-color image signals, optimizing the four-color image signals, and supplying the optimized image signals to the data driver such that the data driver converts the optimized image signals to the data voltages.

Tanioka discloses a device and method comprising:

a plurality of dots (Fig. 2, where 51 is a dot), each dot including red, green, blue, and white pixels (Fig. 2),

the device comprising:

a gate driver (Fig. 7, driver 49) supplying the gate signals to the gate lines;

a data driver (Fig. 7, driver 47) supplying the data voltages to the data lines; and

an image signal modifier (Fig. 1) for converting three-color image signals into four-color image signals (Fig. 1 shows a 3-color signal being converted into a 4-color signal at lines 8), optimizing the four-color image signals (the pseudo-halftone processor 14-1 to 14-3 optimizes the 4-color signal), and supplying the optimized image signals to the data driver such that the data driver converts the optimized image signals to the data voltages (Fig. 1, where R", G", B", and W" are the optimized signals and as seen in Fig. 7, these signals are supplied to the display device and the data driver).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to make the display, in which the data lines have a second portion that has a line width larger than other portions of the lines at every pixel, taught by Kawano et al. have color pixels and a white pixel as well as the signal modifier as taught by Tanioka, such that all of the color pixels and white pixels would have the larger line width portions, in order to provide an image processing apparatus and method which can display a color image with rich colors.

7. Claims 14 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawano et al. (US 6,985,194) in view of Tanioka (US 5,929,843) and further in view of Morita (US 2002/0196243).

Regarding claim 14, Kawano et al. and Tanioka disclose the device of claim 13. Tanioka also discloses a device wherein the image signal modifier comprises:

a data converter converting three-color image signals into four-color image signals (Fig. 1, the section comprising 13-1, 13-2, 13-3, and 11 is a data converter);

a data optimizer optimizing the four-color image signals from the data converter (14-1 to 14-4 is the data optimizer); and

a data output unit supplying the optimized image signals to the data driver (Fig. 7, display controller 44 performs this function).

Kawano et al. and Tanioka fail to teach supplying the image signals to the data driver in synchronization with a clock; and a clock generator generating the clock, the data driver operating in synchronization with the clock.

Morita discloses a liquid crystal display where supplying the image signals to the data driver is in synchronization with a clock (see para. 239); and a clock generator generating the clock (see para. 239, where there is a control signal generation circuit 74 providing the clock), the data driver operating in synchronization with the clock (para. 239).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Morita in the device of Kawano et al. and Tanioka in order to have a device where the data driver received image signal at the same rate it output data signals to the display.

Regarding claim 18, Kawano et al., Tanioka and Morita disclose the device of claim 14.

Tanioka also discloses wherein the data output unit outputs the optimized image signals by group of four optimized image signals (Figure 7 and column 4, lines 63-65 explain that the display controller 44 reads out the RGB and W binary data from the frame memory and supplies them to a shift register in a serial manner.).

Allowable Subject Matter

8. Claims 15-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Relative to dependent claim 15, the major difference between the prior art of record (Tsutomu, Tanioka, Kawano et al.) and the instant invention, is that the prior art does not teach optimized image signals determined by: W'=Min(W.sub.0, 255); R'=R.sub.0+Max(0, W.sub.0-255); G'=G.sub.0+Max(0, W.sub.0-255); and B'=B.sub.0+Max(0, W.sub.0-255).

Regarding dependent claim 16, the major difference between the prior art of record (Tsutomu, Tanioka, Kawano et al.) and the instant invention, is that the prior art does not teach optimized image signals determined by: G'=G.sub.0+(255-Max(R.sub.0,

G.sub.0, B.sub.0)); and B'=B.sub.0+(255-Max(R.sub.0, G.sub.0, B.sub.0)), (**Note the claim objection above regarding this claim. The preceding analysis using "B'" and "B.sub.0" was how the claim was best understood to be intended by the applicant).

Relative to dependent claim 17, the major difference between the prior art of record (Tsutomu, Tanioka, Kawano et al.) and the instant invention, is that the prior art does not teach optimized image signals determined by: W'=(W.sub.0+Average(R.sub.0, G.sub.0, B.sub.0))/2; R'=R.sub.0+(W.sub.0-Average(R.sub.0, G.sub.0, B.sub.0))/2; G'=G.sub.0+(W.sub.0-Average(R.sub.0, G.sub.0, B.sub.0))/2; and B'=B.sub.0+(W.sub.0-Average(R.sub.0, G.sub.0, B.sub.0))/2.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Isami et al. (US 7,164,403) disclose of data lines for a display which have a first portion and a second portion which both have larger line widths than the other portions of the data lines (Figure 22).

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SS

27 August 2007

AMR A. AWAD
SUPERVISORY PATENT EXAMINER